REMARKS

The drawings are objected to as not showing the capacitor set forth in claims 8 and 9. The drawings are further objected to as failing to show a capacitor as described in the specification. Figure 9 is amended herein to clearly illustrate the capacitor in one embodiment of the voltage compensating circuit 930 of the invention. The capacitor is described in the specification as filed at least at page 9, line 32 through page 10, line 2. Accordingly, the amendment to Figure 9 does not introduce new matter into the application.

It is believed that the objections to the drawings are overcome, and reconsideration is requested.

Claims 1-10 are rejected under 35 U.S.C. § 102(e) as being anticipated by Nguyen (U.S. Patent Number 6,429,686). In view of the amendments to the claims and the following remarks, the amendments are respectfully traversed, and reconsideration of the rejections is requested.

The claims are amended herein to clearly set forth features of the semiconductor memory device of the applicants' invention. Specifically, claims 1-3 are amended to set forth the first driving circuit for receiving a reference voltage and generating a first internal voltage and a second driving circuit for receiving an internal supply voltage and data and generating a second internal voltage. The claims are further amended to set forth that the first and second internal voltages are applied to the gates of the first and second NMOS transistors, respectively, of the invention.

These amendments clarify patentable distinctions between the applicants' invention and the cited Nguyen patent. For example, referring to Figure 3A of Nguyen and its corresponding description, there is neither taught nor suggested a first driving circuit that receives a reference voltage and generates a first internal voltage applied to the gate of a first NMOS transistor. Further, there is neither taught nor suggested a second driving circuit that receives an internal supply voltage and data and generates a second internal voltage that is applied to the gate of the second NMOS transistor. Accordingly, the invention set forth in the amended claims 1-3 is neither taught nor suggested by Nguyen. Accordingly, it is believed that claims 1 through 3 are allowable over Nguyen.

With regard to claims 4-6, they have been amended to clarify the invention. Claims 4-6 recite that a ground voltage level of the driving circuit is higher than the voltage level of the ground voltage to which the source of the second NMOS transistor is connected. This feature of the invention set forth in claims 4-6 is neither taught nor suggested by Nguyen. Nguyen neither teaches nor suggests two different ground voltage levels. It also neither teaches nor suggests a driving circuit ground voltage level being higher than a ground voltage to which the source of a second NMOS transistor is connected. Accordingly, Nguyen fails to teach or suggest the invention set forth in claims 4-6 and, therefore, it is believed that claims 4-6 are allowable over Nguyen.

With regard to claims 7-10, they have also been amended to clarify distinctions between the invention set forth therein and the Nguyen reference. Specifically, the claims have been amended to clarify the precharge transistor of the invention. That is, claim 7 is amended to clarify that the precharge transistor is connected to the voltage compensating circuit. Other clarifying amendments are made to the claim to clarify that the semiconductor memory device of the invention includes an output driver in the precharge transistor.

The Nguyen reference fails to teach or suggest the applicants' claimed voltage compensating circuit. The Office Action refers to Nguyen at Column 6, lines 53-55, for disclosure of this claimed subject matter. However, the applicants have reviewed the entire Nguyen patent, specifically the portions referred to in the Office Action, and can find no such teaching or suggestion. Furthermore, the Office Action refers to item 212 in Figure 2 of Nguyen as teaching the applicants' claimed capacitor. It is true that item 212 is a capacitor. However, it is not a voltage compensating circuit connected between the gate and the source of a precharge transistor. The Examiner refers to Nguyen's disclosed pull-up transistor 405B in Figure 4 as the applicants' claimed precharge transistor. Assuming only for the sake of this discussion that Nguyen's pull-up transistor 405B is the applicants' claimed precharge transistor, Nguyen's capacitor 212 shown in Figure 2 is clearly not connected to Nguyen's transistor 405B shown in Figure 4 between its source and gate, as set forth in the applicants' claims. Accordingly, Nguyen fails to teach or suggest the invention set forth in amended claims 7-10.

Nguyen fails to teach or suggest the invention set forth in amended claims 1-10. Accordingly, it is believed that the amended claims are allowable over Nguyen, and reconsideration of the rejections of claims 1-10 under 35 U.S.C. § 102(e) based on Nguyen is respectfully requested.

In view of the amendments to the claims and the foregoing remarks, it is believed that all claims pending in the application are in condition for allowance, and such allowance is respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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Amendments to the Drawings:

The attached sheet of drawings includes changes to FIG. 9. The sheet, which includes FIGs. 9 and 10, replaces the original sheet. FIG. 9 is amended to illustrate the capacitor of the invention.

A marked-up version of the drawings, with revisions shown in red, is included with the amended drawings. Entry of the amendments to the drawings is respectfully requested.

Attachment: Replacement Sheet
Annotated Sheet Showing Changes

FIG. 9

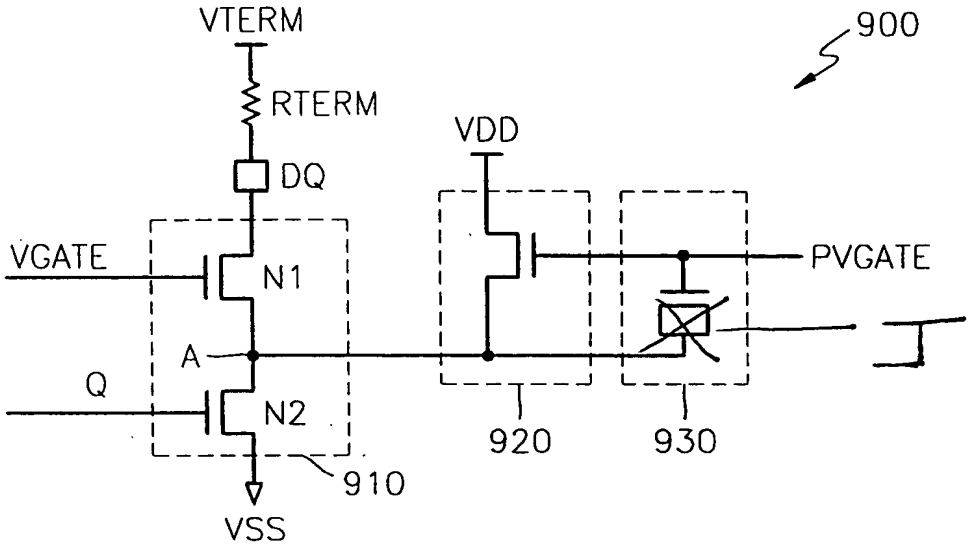
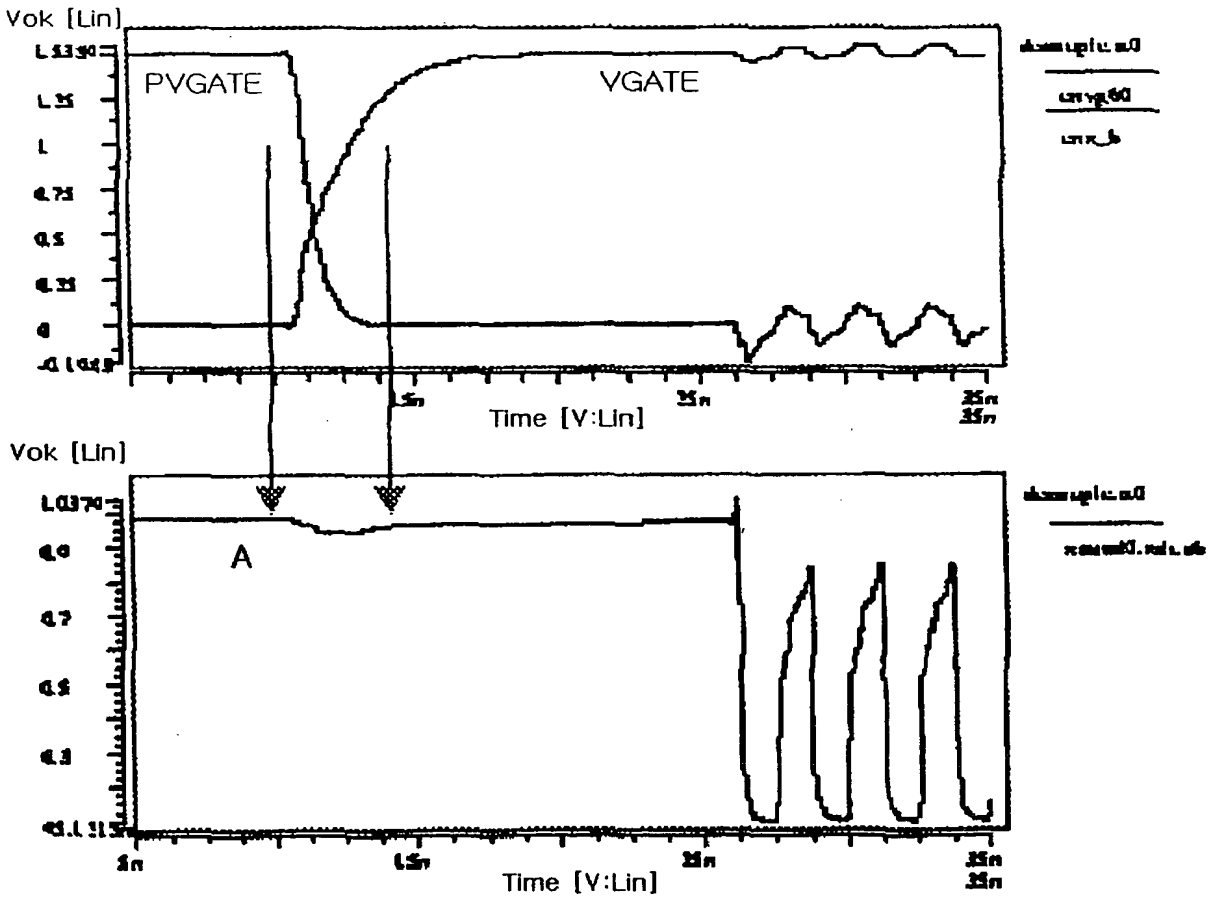

VTERM
RTERM
DQ
VGATE
N1
A
Q
N2
VSS
910
VDD
920
930
PVGATE
900

FIG. 10


Vok [Lin]
PVGATE
VGATE
Time [V:Lin]
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Time [V:Lin]